AF/2823

Docket No.: 50099-180

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of	:	Customer Number: 20277
Shigenobu MAEDA, et al.	:	Confirmation Number: 8927
Application No.: 09/988,593	:	Group Art Unit: 2823
Filed: November 20, 2001	:	Examiner: T. Pham

For: SEMICONDUCTOR DEVICE HAVING IMPURITY REGION UNDER ISOLATION REGION (As Amended)

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith in triplicate is Appellants' Appeal Brief in support of the Notice of Appeal filed September 9, 2003. Please charge the Appeal Brief fee of $330.00 to Deposit Account 500417.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Sir:

This Appeal Brief is submitted in support of the Notice of Appeal filed September 9, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is Mitsubishi Denki Kabushiki Kaisha.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals and interferences.

III. STATUS OF CLAIMS

Claims 1-24 are pending in this application. Claims 10-24 have been withdrawn from consideration pursuant to the provision of 37 C.F.R. § 1.142(b), and claims 1-9 have been finally rejected. It is from the final rejection of claims 1-9 that this Appeal is taken.

IV. STATUS OF AMENDMENTS

An Amendment was submitted pursuant to 37 C.F.R. § 1.116 on July 7, 2003, subsequent to the imposition of the Final Office Action dated April 10, 2003. In the Advisory Action dated July 22, 2003, the Examiner indicated that the Amendment of July 7, 2003, would be entered if an Appeal is taken. As an Appeal has been taken, Appellants are proceeding on the basis that the Amendment of July 7, 2003 has been entered.

V. SUMMARY OF INVENTION

The present invention addresses and solves the problems flowing from source/drain impurity ions 19 being deposited into a well region 11 below a partial oxide film 31 (page 2 of Appellants' disclosure, lines 14-18; Fig. 33). These impurities can change the resistance value of the body resistance R1 of the well region 11, which causes the threshold voltage of the resistor to disadvantageously fluctuate and cause unstable operation of the transistor (page 4, line 19 through page 5, line 2). To prevent the well region 11 from being implanted with the source/drain impurity ions 19, one approach that has been considered is to increase the thickness of the partial oxide film 31 (page 3, lines 10-19). However, if such an approach is undertaken, residue 33 is left on the partial oxide film 31 (page 3, lines 20-21; Fig. 35). Although this residue

33 may be removed by increased etching, the increased time of etching can disadvantageously result in damage to a gate oxide film 8 adjacent the partial oxide film 31 (page 3, lines 21-23). Therefore, there was a need for an improved semiconductor device that controls body resistance in more stable manner.

According to the present invention, the above body resistance fluctuation problem is solved by forming a first conductivity semiconductor region under an isolation film that at least partially has a region doped by only an impurity of a first conductivity type, as recited in independent claim 1. Since the first conductivity type impurity region does not include second conductivity type impurities, the resistance value of the body resistance can be reduced and dispersion can be suppressed (page 23, lines 10-14). Consequently, a precisely controllable semiconductor device having a partially isolated body fixed SOI structure can be obtained without increasing the resistance value of the body resistance (page 23, lines 14-16). The present invention, thus, constitutes an improvement over conventional semiconductor devices by providing a region under an isolation film that includes impurities of one conductivity type but not of another conductivity type.

VI. ISSUE

A. The Rejection:

1. Claims 1-9 are rejected under 35 U.S.C. § 102 for lack of novelty based upon Flaker et al., U.S. Patent No. 6,410,369.

B. The Issue Which Arises In This Appeal And Requires Resolution By The Honorable Board of Patent Appeals And Interferences (The Board) Is:

1. Whether claims 1-9 are unpatentable under 35 U.S.C. § 102 for lack of novelty based upon Flaker et al., U.S. Patent No. 6,410,369.

VII. GROUPING OF CLAIMS

The appealed claims do not stand or fall together. Claims 1-6 stand or fall together as a group with claim 1, and claims 7-9 stand or fall together as a group with claim 7.

VIII. THE ARGUMENT

Initially, Appellants note that in the Final Office Action dated April 10, 2003, the Examiner objected to claim 10 (third enumerated paragraph on page two) and the Examiner rejected claims 1-9 under 35 U.S.C. § 103 for obviousness based upon Flaker in view of Ooishi et al. However, the Examiner stated in the Advisory Action dated July 22, 2003, that the rejection of the claims based upon Ooishi is withdrawn. Also, since Appellants cancelled claim 10 in the Amendment filed July 7, 2003, the objection to claim 10 is moot.

Furthermore, in the Final Office Action dated April 10, 2003, the Examiner rejected claim 1 under the first paragraph of 35 U.S.C. § 112. However, in the Advisory Action dated July 22, 2003, the Examiner stated that the rejection of claim 1 under the first paragraph of 35 U.S.C. § 112 has been overcome by Appellants.

The Rejection of Claims 1-9 under 35 U.S.C. § 102 for Anticipation based upon Flaker et al., U.S. Patent No. 6,410,369 (hereinafter Flaker)

The Examiner has rejected claims 1-9 for anticipation based upon Flaker in both the initial Office Action dated December 13, 2002, and in the Final Office Action dated April 10, 2003. In response to both Office Actions, Appellants argued that Flaker fails to identically disclose the following limitation found in independent claim 1:

> said semiconductor region at least partially has a first conductivity type impurity region not mixed with an impurity of a second conductivity type different from said first conductivity type but doped by only an impurity of said first conductivity type.

The claimed semiconductor region is shown, for example, as features 11, 12 in Fig. 1 of Appellants' disclosure. In both Office Actions, the Examiner referred to "(body link, Fig. 10B)" of Flaker as disclosing a first conductivity type region of the semiconductor region corresponding to that claimed. This feature is labeled with reference numeral 32 in Fig. 10B of Flaker.

In the Amendment filed March 10, 2003, Appellants argued that the body link 32 of Flaker does not correspond to the claimed semiconductor regions that is doped by only an impurity of a first conductivity type. This argument is reproduced below:

> Furthermore, the Examiner identified a "body link 32" in Figs. 8 and 10B of Flaker as corresponding to the first conductivity type semiconductor region recited in claim 1. The body link 32 of Flaker is provided in a silicon layer of a P-type (first conductivity type), so that the body [link] 32 contains P-type impurities. However, according to Flaker, a surface of a portion of the silicon layer where the body link 32 is to be formed is covered with oxide films 52, 56 during a process of implanting arsenic ions, as shown in Fig. 13, and it is almost impossible to completely prevent arsenic ions from being introduced into the portion where the body link 32 is to be formed by only providing the oxide films 52, 56. As such, in the process shown in Fig. 13, arsenic ions would inevitably be introduced into the portion where the body link 32 is to be formed. Thus, the body link 32, as formed, would contain N-type (second conductivity type) impurities, as well as P-type impurities.
>
> In contrast, the recited semiconductor region includes a first conductivity type impurity region formed of only first conductivity impurities. According to the present invention, a N^+ block region 41 is provided in a N^+ block resist 51 during implantation of N-type impurities to thereby

> obtain the first conductivity type impurity region, for example, as shown in Figs. 10 and 11. The provision of the N^+ block region 41 completely prevents N-type impurities from being introduced into a portion of a well region 11 (corresponding to the recited semiconductor region in claim 1) located under the N^+ block region 41. As a result, a P-type impurity region (corresponding to the first conductivity type impurity region in claim 1), which is not mixed with a N-type impurity, will be formed in the portion of the well region 11 located under the N^+ block region 41. Flaker neither discloses or suggests a process for obtaining a region formed of only P-type impurities, as it is impossible to arrive at the semiconductor region recited in claim 1 from the teachings of Flaker.

The Examiner responded to this argument in the twelfth enumerated paragraph of the Final Office Action with the following statement:

> In response to applicants' argument in the paragraph bridged pages 8 and 9 that the portion of the body link 32 would contain both type of impurities and the description of the instant invention of the next paragraph, applicants are directed to col. 6, lines 7-23 wherein the reference assures a precise control of the forming of element 62, therefore, no mixed impurities would exist in the body link 32.

For ease of analysis, the Examiner's cited passage of column 6, lines 7-23 of Flaker is reproduced below:

> A shallow N+(As) implant 58 is then made into the areas 60 not protected by the nitride pad or the CVD oxide (FIG. 13). The structure then goes through a high-pressure, low-temperature oxidation (HIPOX) cycle. The N+ regions 60 (formed in FIG. 13) oxidize without appreciable diffusion to form HIPOX regions 62. That is, oxidation proceeds rapidly through the N+ regions, then slows dramatically in the P-type silicon, without significant As dopant outdiffusion. Experiments have shown that a 700°C., HIPOX oxidation can result in the N+ layer oxidizing greater than five (5) times faster than the underlying P-type silicon. This allows very precise control of the oxidation depth, since the oxidation rate will slow markedly when the shallow N+ region is consumed (FIG. 14). This step and the particular type of control is critical for assuring that body links will have good continuity yield.

In the Amendment filed July 7, 2003, Appellants argued that this cited passage does not provide any teaching that the body link 31 does not include a portion having no impurities of the second conductivity type (i.e., N-type impurities in Flaker). Appellants also argued that the Examiner's argument that the "very precise control of the oxidation depth" somehow corresponds to no mixed impurities is unpersuasive because the Examiner has not provided any necessary link between precise control of oxidation depth, as indicated by Flaker, and the claimed limitation of a region "doped by only an impurity of said first conductivity type."

In responding to these arguments, the Examiner stated the following in the Advisory Action dated July 22, 2003:

> Continuation of 5. does NOT place the application in condition for allowance because: Applicant argues that Flaker fails to identically disclose the claimed feature of the last limitation in claim 1 in which Flaker's body link 31 does not include a portion having no impurities of the second conductivity type. The reference discloses removal of the shallow doped region through oxidation or through selective etching to leave the p-type conductive link. Applicant has not established that there would not be a portion of the link region which does not contain n-type dopants. (emphasis added)

Appellants note that the Examiner has not contested Appellants' arguments that Flaker fails to identically disclose the limitation of "doped by only an impurity of said first conductivity type," since Flaker is silent as to this particular feature. Although not specifically invoking the doctrine of inherency, the Examiner has responded to this deficiency in Flaker by arguing that the process of Flaker would inherently remove the N-type dopants, thereby leaving only the p-type conductive link.

Appellants respectfully submit that the Examiner's implied reliance upon the doctrine of inherency to disclose the limitation of "doped by only an impurity of said first conductivity type" is misplaced. Inherency may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient to establish inherency.[1] To establish inherency, the extrinsic evidence must make clear that the missing element must necessarily be present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill.[2]

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[1] In re Rijckaert, 9 F.3d 1531, 28 USPQ2d 1955 (Fed. Cir. 1993) (reversed rejection because inherency was based on what would result due to optimization of conditions, not what was necessarily present in the prior art); In re Oelrich, 666 F.2d 578, 212 USPQ 323, (CCPA 1981).

[2] Finnegan Corp. v. ITC, 180 F.3d 1354, 51 USPQ2d 1001 (Fed. Cir. 1999); In re Robertson, 169 F.3d 743, 49 USPQ2d 1949 (Fed. Cir. 1999); Continental Can Co. USA v. Monsanto Co., 20 USPQ 2d 1746 (Fed. Cir. 1991); Ex parte Levy, 17 USPQ2d 1461 (BPAI 1990).

As reproduced above and previously argued in the Amendment filed March 10, 2003, Appellants have argued that the process of Flaker would introduce N-type impurities into the body link 32, as well as P-type impurities, and thus, the body link 32 of Flaker fails to meet the claimed limitation at issue. Furthermore, contrary to the Examiner's assertion in the Advisory Action that "Applicant has not established that there would not be a portion of the link region which does not contain n-type dopants," the burden is on the Examiner to establish a prima facie case of anticipation. Even if the Honorable Board decides to give no weight to Appellants' arguments that the process of Flaker would introduce both N-type and P-type impurities into the body link 32, the Examiner has still failed to establish that the claimed feature of "doped by only an impurity of said first conductivity type" would necessarily be disclosed by Flaker.

Appellants separately argue the rejection of claims 7-9 for lack of novelty based upon Flaker. In the Final Office Action dated April 10, 2003, the Examiner stated the following:

> With respect to claims 7-9, there are regions on the wafer of the reference that are not active regions and could therefore be labeled as "dummy regions."

The term "dummy" has a specific meaning when used in the semiconductor art. Specifically, this term refers to a specific feature(s) or structure(s) that is identical or nearly identical to an operational feature or structure but the dummy feature or structure is non-operational. The Examiner's use of the term "active" to describe a dummy region is ambiguous because the term "active" could be synonymous with an operational device or, as commonly used in the semiconductor art, the term "active" could be used to describe a doped region, such as a source or a drain, and these two meanings are not identical. Notwithstanding the Examiner's ambiguous use of the term "not active region," Appellants note that the Examiner has failed to establish

where these regions are disclosed by Flaker. The Examiner has neither cited a passage, pointed to a drawing, nor identified a reference numeral in Flaker where a teaching regarding the "not active region" can be found. Thus, Appellants submit that Flaker fails to disclose the claimed dummy region within the meaning of 35 U.S.C. § 102.

IX. CONCLUSION

It should, therefore, be apparent that the Examiner did not discharge the initial burden of establishing a prima facie case of anticipation under 35 U.S.C. § 102. The above argued differences between the semiconductor device defined in independent claim 1 and the device of Flaker undermine the factual determination that Flaker identically describes the claimed invention within the meaning of 35 U.S.C. § 102. Furthermore, the Examiner has failed to establish that the features not identically disclosed by Flaker are inherently disclosed. Appellants, therefore, respectfully submit that the imposed rejection of claims 1-9 under 35 U.S.C. § 102 for anticipation based upon Flaker is not factually viable. Appellants submit that the Examiner has also failed to establish that the claim 1 does not include a "critical feature," and thus, the Examiner's rejection of claim 1 under the first paragraph of 35 U.S.C. § 112 is improper.

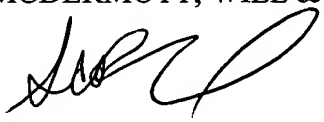
X. PRAYER FOR RELIEF

Based upon the foregoing, Appellants respectfully submit that one having ordinary skill in the art would not have found the claimed invention anticipated within the meaning of 35 U.S.C. § 102. Appellants, therefore, respectfully solicit the Honorable Board to reverse the Examiner's rejections under 35 U.S.C § 102 and the first paragraph of 35 U.S.C. § 112.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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APPENDIX

1. A semiconductor device having an SOI structure formed by a semiconductor substrate <1>, an embedded insulating layer <2> and an SOI layer <3>, comprising:

a plurality of element forming regions provided in said SOI layer, each formed with a prescribed element;

an isolation film <31> provided in an upper layer part of said SOI layer for isolating said plurality of element forming regions from each other;

a first conductivity type semiconductor region <11, 12> provided under said isolation film as part of said SOI layer, said semiconductor region being formed in contact with at least one of said plurality of element forming regions having a first conductivity type among said plurality of element forming regions; and

a first conductivity type body region <10> provided in said SOI layer and capable of being externally fixed in electric potential, said body region being in contact with said semiconductor region, wherein

said semiconductor region at least partially has a first conductivity type impurity region not mixed with an impurity of a second conductivity type different from said first conductivity type but doped by only an impurity of said first conductivity type.

2. The semiconductor device according to claim 1, wherein

said first conductivity type impurity region is formed in a region <36> reaching said at least one element forming region from said body region.

3. The semiconductor device according to claim 1, wherein

said isolation film at least partially has a second conductivity type impurity-free region containing no impurity of said second conductivity type.

4. The semiconductor device according to claim 3, wherein

said second conductivity type impurity-free region is formed in a region reaching said at least one element forming region from said body region.

5. The semiconductor device according to claim 3, wherein

said second conductivity type impurity-free region includes a region having a larger thickness than the remaining region in said isolation film.

6. The semiconductor device according to claim 1, wherein

said prescribed element includes a transistor, and a gate electrode <9> of said transistor is formed to extend on said isolation film.

7. The semiconductor device according to claim 1, wherein

a dummy region <73, 74> formed in said SOI layer not to function as an element.

8. The semiconductor device according to claim 7, wherein

said dummy region includes a region where impurities of both of said first conductivity type and said second conductivity type are introduced.

9. The semiconductor device according to claim 7, wherein

said dummy region includes a first dummy region <72> where an impurity of said first conductivity type is implanted and no impurity of said second conductivity type is implanted and a second dummy region <71> where an impurity of said second conductivity type is implanted and no impurity of said first conductivity type is implanted.